Ayukawa 1-4-1-162-30

ALUMINUM PAD POWER BUS AND SIGNAL ROUTING FOR INTEGRATED CIRCUIT DEVICES UTILIZING COPPER TECHNOLOGY INTERCONNECT STRUCTURES

[0001] This patent application claims the benefit of the provisional patent application filed on April 10, 2003, assigned application number 60/462,504 and entitled Aluminum Pad Power Bus in a Copper Technology.

BACKGROUND OF THE INVENTION

[0002] Integrated circuits (or chips) typically comprise a silicon substrate and semiconductor devices, such as transistors, formed from doped regions within the substrate. Interconnect structures, formed in parallel-like layers overlying the semiconductor substrate, provide electrical connection between devices to form electrical circuits. Typically, several (e.g., 6-9) interconnect layers (each referred to as an "M" or metallization layer) are required to interconnect the devices in a typical integrated circuit. The top interconnect layer comprises a plurality of pads that serve as attachment points for conductive elements (e.g.., bond wires or solder balls) for interconnecting the integrated circuit devices to off-chip external contacts, such as pins or leads of a package structure.

[0003] A conventional interconnect system comprises a plurality of substantially vertical conductive vias or plugs and substantially horizontal conductive interconnect layers, with a dielectric layer disposed between two vertically adjacent interconnect layers. Upper level conductive vias interconnect two vertically adjacent interconnect layers. Conductive vias in the first or lowest level interconnect an underlying semiconductor device region to an overlying interconnect layer. The interconnect structures are formed by employing conventional metal deposition, photolithographic masking, patterning and etching techniques.

[0004] As integrated circuit devices and interconnect structures shrink, and as the devices carry higher frequency analog signals and higher data rate digital signals, the interconnect structures can disadvantageously add delays to the signal propagation time. Also, the increasing complexity of the devices and the added functionality they provide

may require a greater number of interconnect structures or levels. But the conventional interconnect metallization material, e.g., aluminum, severely limits signal speed. Also, the contact resistance between the aluminum interconnect structure and device silicon regions contributes significantly to the total circuit resistance, especially as the number of circuit devices and interconnect structures increases. Finally, as interconnect line widths shrink, it is increasingly difficult to deposit conductive material in openings or windows to form high aspect ratio (i.e., the ratio of the opening depth to the opening diameter) conductive vias.

[0005] Given the known disadvantages of aluminum interconnect structures, copper is becoming the interconnect material of choice. Copper is a better conductor than aluminum (with a resistance of 1.7 micro-ohm cm compared to 3.1 micro-ohm cm for aluminum), is less susceptible to electromigration (a phenomenon whereby the aluminum interconnect structure thins and can eventually separate due to the electric field and thermal gradients formed by current flow through the aluminum interconnect), can be deposited at lower temperatures (thereby avoiding deleterious effects on previously formed dopant profiles) and is suitable for use in high aspect ratio applications.

[0006] The damascene process is one technique for forming copper interconnect structures for integrated circuit devices. Typically, the copper damascene process integrally forms both the conductive vertical via portion and the conductive horizontal interconnect portion (referred to as a metal runner) of an interconnect or metallization layer. To form a copper damascene structure, a hole or window is formed in a dielectric layer, followed by formation of an overlying trench for the metal runner. A subsequent metal deposition step fills both the opening and the trench, forming a complete metal layer comprising a substantially vertical conductive via and a substantially horizontal conductive runner. A final chemical/mechanical polishing step planarizes the deposited metal with respect to the adjacent surface of the dielectric layer.

[0007] An example of a prior art dual damascene process is illustrated in the cross-sectional views of Figures 1A-1C during various stages of fabrication. As depicted in Figure 1A, a dielectric layer 10 is deposited or formed on lower level interconnect 12. A photoresist layer 16, formed over the dielectric layer 10, is patterned and etched according to conventional techniques to form an opening 18 therein. An anisotropic etch process etches a via hole or window 20 in the dielectric layer 10 through the opening 18. The photoresist layer 16 is removed and replaced by a photoresist layer 30

(see Figure 1B) that is then patterned and etched to form a trench pattern 32. An anisotropic etch process forms a trench 34 (extending perpendicular to the plane of the paper) and simultaneously extends the opening 18 to an upper surface 36 of the lower level interconnect 12. The hole or window 20 can be formed to stop on the upper surface 36 and expose the lower level interconnect 12 (as shown in Figure 1B) or alternatively can be over-etched to extend partially into the lower level interconnect 12.

[0008] As illustrated in Figure 1C, the hole 20 and trench 34 are simultaneously filled with a suitable conductive material 40, such as copper. According to standard process techniques, a copper seed layer is first deposited, followed by copper electroplating to fill the hole 20 and the trench 34. The material 40 thus forms a conductive trench 42 and a conductive via 44 in contact with the lower level interconnect 12. Additionally, if the material 40 comprises copper, a barrier layer, such as a tantalum layer and/or a tantalum-nitride layer (or other refractory materials and their nitrides) is deposited in the hole 20 and the trench 34, prior to copper deposition. The barrier layer or layers prevents the diffusion of copper into the surrounding material of the dielectric layer 10. Finally, after deposition, the surface of the dielectric layer 10 is planarized to remove excess metal 40 from a field region 48 using techniques, such as chemical/mechanical polishing (CMP), that are well known in the art.

[0009] A second example of prior art dual damascene structure for integrated circuit devices is shown in Figures 2A-2C. As depicted in Figure 2A, multiple material layers are formed on a lower level interconnect 58, including a first etch stop layer 60, a first dielectric layer 62, a second etch stop layer 64, a second dielectric layer 66, and an etch mask 68. The etch mask 68 is patterned and etched to form an opening 70 therein. Using the etch mask pattern, an anisotropic first etch process forms a via opening 72 in the second dielectric layer 66, extending downwardly through the second etch stop layer 64 to the first etch stop layer 60. The etch process is terminated when the etchant reaches the etch stop layer 60. The etch mask 68 is removed, an etch mask 78 (see Figure 2B) is positioned over the second dielectric layer 66 and masked to form an opening 79, which is larger laterally than the opening 70. A second anisotropic etch process etches a trench 80 in the second dielectric layer 66. Simultaneously, the via opening 72 is extended downwardly by etching through the etch stop layer 60, to contact with the underlying lower level interconnect 58. According to this technique the first etchant has a greater selectivity to the etch stop layer 60 than the second etchant. To

complete the damascene process, the mask 78 is removed and the trench 80 and via opening 72 are simultaneously filled with a suitable conductive metal (see Figure 2C) forming a conductive runner 88 and a conductive via 90 in contact with the lower level interconnect 58. The excess conductive material is removed from a field region surface 92 of the second dielectric layer 66, using techniques such as CMP, as known in the art.

[0010] In addition to carrying signals between the semiconductor elements, the interconnect structure, whether fabricated from aluminum or copper, is also required to supply power to the various device elements through a power bus structure. In most integrated circuits the power bus is formed as an additional interconnect layer, including vertical conductive vias and a horizontal interconnect layer. Typically the power bus forms the top level interconnect structure. Disadvantageously, the additional power bus interconnect layer increases the number of mask steps, mask layers and process steps, all contributing to an increased fabrication cost. Further, these additional process steps can lower the device yield as they present opportunities for the occurrence of processing defects.

[0011] Since the power bus conducts a relatively high current, as compared with the signal interconnect structures, the power bus interconnect layer generally has a greater width, thickness and pitch than the signal interconnect layers. The power bus is also a source of noise and parasitic capacitance that can disrupt performance of proximate devices and interconnect structures. To limit these effects, the power bus may be isolated from other device structures, with the isolating structures consuming valuable device area.

BRIEF SUMMARY OF THE INVENTION

[0012] An integrated circuit device comprises a multilevel interconnect metallization system formed over a semiconductor substrate layer, wherein the metallization system includes a bond pad level and one or more levels of interconnect underlying the bond pad level. The bond pad level comprises a plurality of contact pads each configured for connection external to the device and an interconnect configured to transfer power from one or more of the pads to one or more of the underlying levels of interconnect.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] The present invention can be more easily understood and the advantages and uses thereof more readily apparent, when considered in view of the following detailed description when read in conjunction with the following figures wherein:

[0014] Figures 1A-1C and 2A-2C illustrate, in a cross-sectional views taken along a common plane, a prior art dual damascene structure.

[0015] Figure 3 is a perspective cut-away view of a package for an integrated circuit device constructed according to the teachings of the present invention.

[0016] Figure 4 illustrates a prior art flip-chip integrated circuit device structure.

[0017] Figure 5 illustrates, in a cross-sectional view taken along a common plane, a prior art interconnect structure including a power bus.

[0018] Figures 6-11 are cross-sectional views taken along a common plane, illustrating sequential processing steps in the fabrication of an interconnect structure, including a power bus, according to the teachings of the present invention.

[0019] Figure 12 is a top view of a prior art interconnect structure for an integrated circuit device.

[0020] Figure 13 is a top view of an interconnect structure constructed according to the teachings of the present invention.

[0021] In accordance with common practice, the various described device features are not drawn to scale, but are drawn to emphasize specific features relevant to the invention. Reference characters denote like elements throughout the figures and text.

DETAILED DESCRIPTION OF THE INVENTION

[0022] Before describing in detail the particular aluminum pad power bus or signal routing technology for integrated circuit devices in accordance with the present invention, it should be observed that the present invention resides primarily in a novel and non-obvious combination of elements and method steps. Accordingly, these elements and steps have been represented by conventional elements and steps in the drawings, showing only those specific details that are pertinent to the present invention so as not to obscure the description with structural details that will be readily apparent to those skilled in the art having the benefit of the description herein.

[0023] After fabrication, the integrated circuit is attached to a package structure that includes a chip attach region and a plurality of externally-disposed package leads through

which the integrated circuit is connected to external components. Since the package leads cannot be connected directly to the thin fragile interconnect structures, the chip's final or upper metallization layer, referred to as an aluminum pad layer or a bond pad layer, comprises a plurality of bond or contact pads for connection to the package leads via a conductive lead or wire (typically formed from gold or its alloys) connected between a bond pad and an interior disposed contact of the package lead.

[0024] The bond pads are formed by depositing a metal barrier layer, typically tantalum-nitride, tantalum or titanium nitride, followed by an aluminum layer on an upper surface of the integrated circuit. The aluminum layer undergoes conventional masking, patterning, and etchings steps to define the aluminum bond pads. In one embodiment, an antireflective coating layer is disposed over the aluminum layer to reduce aluminum reflections during the photolithographic process. A material of the antireflective coating layer comprises titanium-nitride or silicon oxynitride. The bond pads are connected to one or more underlying interconnect structures or circuit elements through underlying conductive vias. For those devices in which the interconnect structures are formed from copper, such as by the damascene process described above, the bond pads are conventionally formed of aluminum, as it is known that the gold wires adhere poorly to a copper bond pad.

[0025] Figure 3 illustrates a device package 100 comprising package leads 102. An integrated circuit 104 is affixed within a die attach area 106. Bond pads 110 are formed on an upper surface 112 of the integrated circuit 104, and connected to the package leads 102 by gold wires 114. Generally, the bond pads 110 vary between about 40-80 microns and 50-150 microns in length and width, respectively. Although square bond pads are common, use of rectangular bond pads is also known in the prior art.

[0026] In another known package structure, referred to as flip-chip or bump bonding, the bond wires 114 of Figure 3 are replaced with deposited solder bumps 120 formed on the bond pads 110. See Figure 4A. Connection to a package 122 of Figure 4B is accomplished by flipping the integrated circuit 104 and soldering the bumps 120 to receiving pads 124 on the package 122, that in turn connect to a corresponding package lead. In the example of Figure 4B the package leads comprise a ball 126 in the form of a ball grid array, as is known in the art.

[0027] The metallization layer in which the bond pads 110 are formed is required whether the package leads 102 are connected to the integrated circuit 104 by bond wires

114 or solder bumps 120. According to the teachings of the present invention, the aluminum pad layer comprises both bond or contact pads and power bus or signal routing interconnect structures through which power is distributed to the elements of the integrated circuit device or through which signals are routed in the integrated circuit. Since the aluminum pad layer is always required to form the bond pads 110, no additional process steps, mask steps or metallization levels are added to the fabrication process by the present invention. To the contrary, one metallization level may be deleted. The invention is particularly suitable for use with copper technologies (i.e., damascene interconnect structures) since dual passivation stacks are conventionally formed over the copper interconnect structures prior to deposition of the aluminum for the bond pads. Thus the first dual passivation stack forms an effective insulating dielectric between the underlying top level interconnect structures and the overlying power bus formed in the aluminum pad layer.

[0028] Figure 5 illustrates a cross-sectional view of a conventional prior art interconnect metallization structure for an integrated circuit device, showing only the upper metallization levels 5 and 6 of a six level metal interconnect structure. In this example the interconnect structure comprises a copper dual damascene interconnect structure. Those skilled in the art recognize that the teachings of the present invention can be applied to integrated circuit devices having other than six levels or interconnect structures.

[0029] According to the dual damascene process, a level 5 conductive via 130 and level 5 conductive runners 132 and 134 are simultaneously formed within a via opening and trenches previously formed in dielectric layers 135 and 136, respectively. The conductive via 130 and level 5 conductive runners 132 and 134 can be separated by an etch stop layer 137 that facilitates separate formation of the via opening and the trenches according to conventional dual damascene processing. However, the etch stop layer 137 is not required for functionality of the dual damascene elements. The conductive via 130 is connected to an underlying interconnect structure or circuit element not shown in Figure 5. A dielectric barrier layer 140 (exemplary materials include silicon nitride, silicon carbide or combinations thereof) overlies the dielectric layer 136 and the exposed upper surface of the level 5 conductive runners 132 and 134. The dielectric barrier layer 140 acts as an etch stop for fabrication of the next-level conductive via and serves as a diffusion barrier to prevent surface interdiffusion of copper from the conductive runners

132 and 134 into the dielectric layer 136. An additional barrier layer 141 surrounds the various copper features to prevent lateral copper diffusion into the dielectric material.

[0030] Level 6 conductive vias 142, formed in a dielectric layer 144, are in electrical contact with the underlying level 5 conductive runners 132 and 134. A dielectric barrier layer 145, serving the same purpose as the dielectric barrier layer 140, overlies the dielectric layer 144. A power bus 146 is formed in an oxide layer 148 overlying the dielectric layer 144. According to the dual damascene process described above, the conductive vias 142 and the power bus 146 are formed simultaneously in previously formed via openings and trenches. Note the larger cross-sectional area required for the power bus 146 compared with the level 6 conductive runners 132 and 134. This is preferred as the power bus 146 carries higher currents than the low-current signals carried by the conductive runners 132 and 134.

[0031] A first passivation stack 149, comprising a silicon nitride layer 150, an oxide layer 152 and a silicon nitride layer 154 is formed overlying the power bus 146. The first passivation stack 149 forms the first layer of the dual passivation scheme referred to above. Openings are defined in the first passivation stack 149 by conventional lithographic and plasma etching processes to expose the underlying copper of the power bus 146. A conductive barrier layer 155, comprising, for example, tantalum, titanium nitride or tantalum nitride, is formed over regions of the power bus 146 exposed through the openings in the first passivation stack 149. The conductive barrier layer 155 prevents the intermixing of copper from the power bus 146 and aluminum from the aluminum pads. An aluminum layer (more conventionally an aluminum-copper alloy) is blanket deposited over the barrier layer 155, then masked, patterned and etched to form an aluminum pad 156 within the opening and further in contact with the underlying power bus 146 through the conductive barrier layer 155.

[0032] After formation of the aluminum pad 156, the integrated circuit device is again passivated by a second passivation stack 158, comprising an oxide layer 160 and an overlying silicon nitride layer 161.

[0033] As described above, the aluminum pads serve as connection points between the underlying copper interconnect structures and the bonds wires 114 of Figure 3 or the metal bumps 120 of Figure 4. It is also known in the art that additional under-bond or under-ball/bump metallurgy layers and/or materials may be required above and/or below the aluminum pad 156 to ensure adequate adhesion with the gold bond wire or the

solder ball. When the assembly is complete and the packaged chip is inserted into an operative circuit, the aluminum pad 156 carries power to the elements of the integrated circuit device through the power bus 146.

[0034] The thickness of the various layers illustrated in Figure 5 (which is not to scale) is conventional in the art, and the techniques for forming the various material layers are also well known.

[0035] As Figure 5 illustrates only a region of the interconnect structure, at other locations of the integrated circuit device (not shown), aluminum pads similar to the aluminum pad 156 are connected to underlying conductive runners or conductive vias for carrying signals from the package leads to the underlying structure or for supplying signals from the underlying structure to the package leads.

[0036] Figure 6, showing only the uppermost interconnect level of a damascene interconnect structure, begins a series of cross-sectional views depicting the process steps for forming an interconnect metallization structure for an integrated circuit device according to the teachings of the present invention. The conductive via 130 is formed in the dielectric layer 135 and connected to an underlying interconnect structure or circuit element not shown in Figure 6. Conductive runners 132 and 134 are formed in a dielectric layer 162. In one embodiment the dielectric layer 162 comprises silicon dioxide. The material of the various dielectric layers shown in Figures 6-11 can comprise any of the following, and other suitable materials known in the art: fluro-silicate glass (FSG), oxides, fluorine-doped TEOS, (tetraethyl orthosilicate), low dielectric constant materials, and organo-silicate glass (OSG). Also, the material of the various barrier layers shown and described can comprise silicon carbide, silicon nitride, phosphorous-doped oxide and other materials known in the art.

[0037] As shown in Figure 7, the first passivation stack 149 (comprising the silicon nitride layer 150, the oxide layer 152 and the silicon nitride layer 154) is formed overlying the conductive runners 132 and 134 and the dielectric layer 162. Openings 163 and 165 are defined and formed by conventional lithographic and dielectric etching techniques through the first passivation stack 149.

[0038] A conductive barrier layer 166 is formed over the exposed surface. The barrier layer 166, which typically comprises tantalum-nitride, serves as a glue layer between the underlying material and the aluminum to be formed thereover. The tantalum-nitride also reduces the known electromigration effects encountered in aluminum interconnect

structures and provides a diffusion barrier between the overlying aluminum and the underlying copper.

[0039] An aluminum-copper alloy layer 168 (or in certain embodiments, an aluminum-silicon-copper alloy) is blanket deposited as shown in Figure 8, filling the openings 163 and 165. An aluminum pad 170 is formed within the opening 163 by patterning, masking and etching steps performed on the aluminum layer 168. See Figure 9. A conductive via 172 is formed in the opening 165 in conductive contact with the runner 134.

[0040] The same masking, patterning and etching steps employed to form the aluminum pad 170 also form a power bus 174 in the aluminum layer 168. Also, during the step of forming the power bus 174, signal routing interconnects are formed in the aluminum-copper alloy layer 168. The signal interconnects are not shown in Figure 9 as they are located in other regions of the substrate not illustrated in Figure 9.

[0041] An overlying passivation stack 180 comprises an oxide layer 182 and a silicon nitride layer 184 formed as illustrated in Figure 10. Openings are formed by known techniques in the passivation stack 180 to access the aluminum pad 170 (and other opening not shown in Figure 10 or 11 are formed to access the signal routing interconnects). See Figure 11 for the final structure. The integrated circuit device is now ready for attachment to a package and wire bonding or bump bonding of the aluminum pad 170 to the package leads.

[0042] The formation of the power bus 174 in the aluminum pad layer as taught by the present invention eliminates one metallization layer (i.e., a copper layer when the teachings of the present invention are applied to a copper damascene process) and the attendant process steps and mask requirements. The prior art embodiment of Figure 5 includes a metallization layer, i.e., comprising the conductive vias 142, that is absent in the structure according to the present invention as shown in Figure 11.

[0043] Current integrated circuits are fabricated with aluminum pads having a thickness of about 1 micron or greater. This thickness is sufficient for carrying the power current and thus formation of the power bus 174 in the aluminum pad layer is feasible and easily adapted to present fabrication process steps. The mask created for patterning the aluminum pads according to the prior art can be modified to include patterns for the power bus interconnect structures at little extra expense.

[0044] Figure 12 is an exemplary top view of a region of a prior art integrated circuit illustrating certain interconnect structures on and below a surface of the region. Aluminum pads 190 and 192 are connected to underlying (i.e., one level below) metallization level conductive runners 194 and 196 through vertical conductive vias 198 and 200, respectively. The conductive runners 194 and 196 can represent the power bus 146 in Figure 5. A conductive runner 204 disposed in an interconnect level below the conductive runners 194 and 196 (representative of the conductive runners 132 and 134 of Figure 5) is connected to the conductive runner 196 through a conductive via 206, and further connected to additional underlying interconnect structures and elements through a conductive via 208.

[0045] Figure 13 is an exemplary top view of a region of an integrated circuit device illustrating certain interconnect structures on and below the surface of a device as constructed according to the teachings of the present invention. The teachings of the present invention, as can be appreciated by those skilled in the art, can be applied to an integrated circuit device structure having any number of metal interconnect layers, where "n" represents the top metallization level and the underlying levels are referred to with reference to the n^{th} level., e.g., the n-1 or the n-2 level.

[0046] An aluminum pad 220 forms an integral part of a power bus 221 (formed in metallization level "n," i.e., the uppermost level) for connection to underlying n-1 level conductive runners 222 and 223 through vertical conductive vias 226 and 224. When the aluminum pad 220 is connected to a power source, via the package leads as described above, the power bus 221 (which can be representative of the power bus 174 in Figure 6) transfers or distributes power to the conductive runners 222 and 223, that in turn connect to underlying conductive runners (not shown in Figure 13) for continued distribution of power throughout the integrated circuit. Although the power bus 221 is illustrated as connected only to the n-1 metallization level, this is solely for exemplary purposes, as connection to lower metallization levels can be made through a succession of vertical conductive vias.

[0047] Continuing with Figure 13, an aluminum pad 228 forms an integral part of an interconnect structure 229, that is in turn connected to an underlying n-1 level conductive runner 230 through vertical conductive vias 232, 234 and 236. The n-1 level conductive runner 230 is further connected to an n-2 level conductive runner 238 through a conductive via 240. In one example, the aluminum pad 228 can receive signals

external to the integrated circuit via the package leads, and supply the signals to the appropriate device elements through the various interconnect structures connected to the aluminum pad 228.

[0048] An n-level conductive runner 244 forms an integral part of an aluminum pad 245 and is connected to conductive vias 247 and 248, that are further connected to an underlying conductive runner 250 (in an n-i level, where i = 1 to n-1).

[0049] According to a second embodiment of the present invention, the aluminum pad layer provides interconnect structures for underlying copper layers, wherein the interconnect structures are not connected to a pad. For example, as further illustrated in the device top view of Figure 13, conductive runners 280 and 282 (for example, both disposed in the n-1 level) are connected with an interconnect structure 284 (formed in the aluminum pad layer n), through conductive vias 286 and 288. In another example, the conductive runner 250 and a conductive runner 292 (for example, both disposed in the n-1 level) are connected by an interconnect structure 294 formed in the aluminum pad layer (n), through conductive vias 298 and 296. Thus in addition to providing the power bus interconnect structure as described above, interconnect structures (such as the interconnect structure 274) for underlying copper layers can also be formed in the aluminum pad layer. As a result, an underlying interconnect layer can be eliminated by using the aluminum pad layer to provide an interconnect function.

[0050] While the invention has been described with reference to preferred embodiments, it will be understood by those skilled in the art that various changes may be made and equivalent elements may be substituted for elements thereof without departing from the scope of the present invention. The scope of the present invention further includes any combination of the elements from the various embodiments set forth herein. In addition, modifications may be made to adapt a particular situation to the teachings of the present invention without departing from its essential scope thereof. Therefore, it is intended that the invention not be limited to the particular embodiment disclosed as the best mode contemplated for carrying out this invention, but that the invention will include all embodiments falling within the scope of the appended claims.